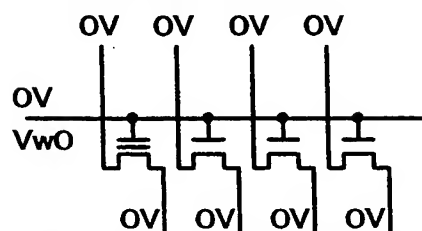


FIG. 1A

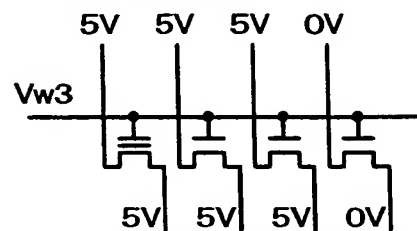
INITIAL STATE



WRITE TARGET DATA	00	01	10	11
MEMORY CELL DATA	00	00	00	00
DISTURBANCE	-	-	-	-

FIG. 1B

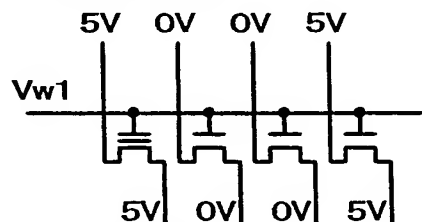
WRITE #1



WRITE TARGET DATA	00	01	10	11
MEMORY CELL DATA	00	00	00	11
DISTURBANCE	++	-	-	-

FIG. 1C

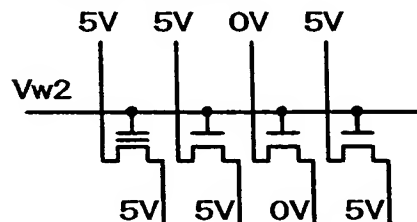
WRITE #2



WRITE TARGET DATA	00	01	10	11
MEMORY CELL DATA	00	01	01	11
DISTURBANCE	++	-	-	+

FIG. 1D

WRITE #3



WRITE TARGET DATA	00	01	10	11
MEMORY CELL DATA	00	01	10	11
DISTURBANCE	++	++	-	+

FIG. 1E

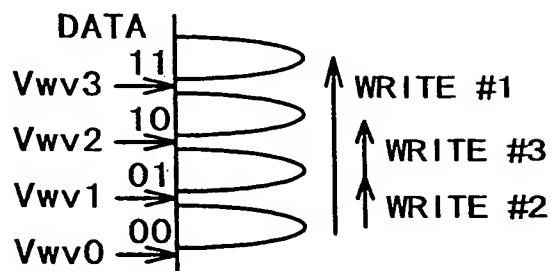


FIG. 2A

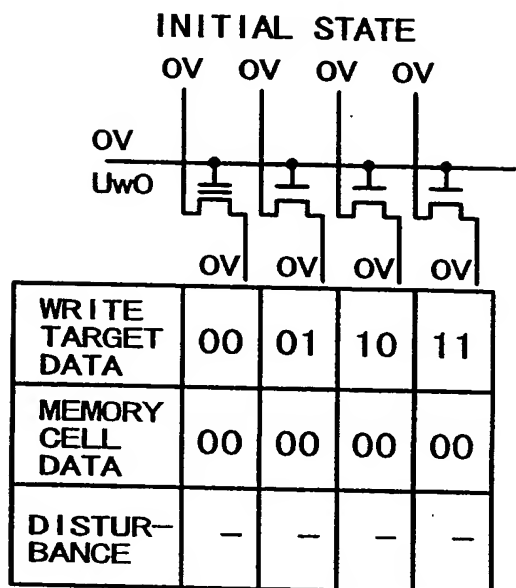


FIG. 2B

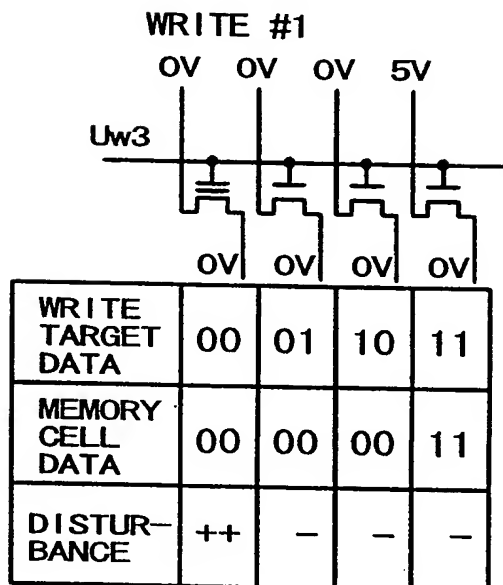


FIG. 2C

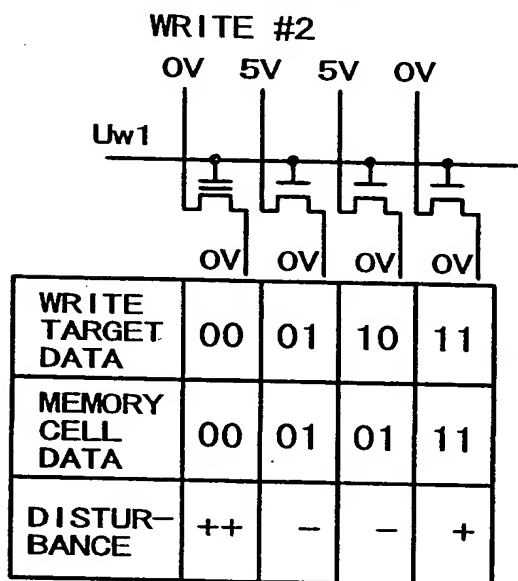


FIG. 2D

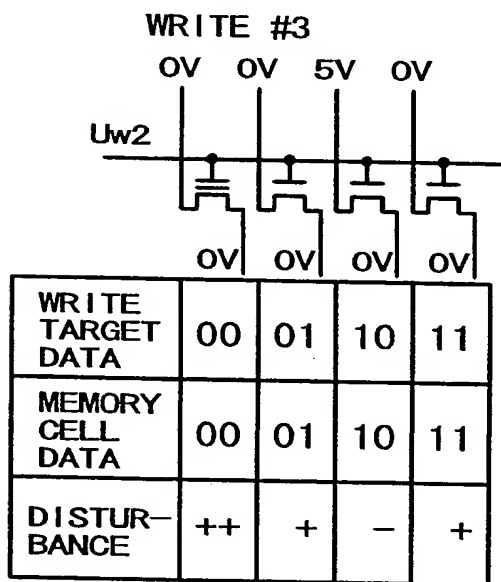


FIG. 2E

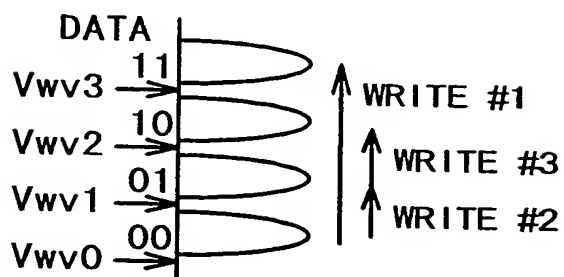


FIG. 3A (PRIOR ART)

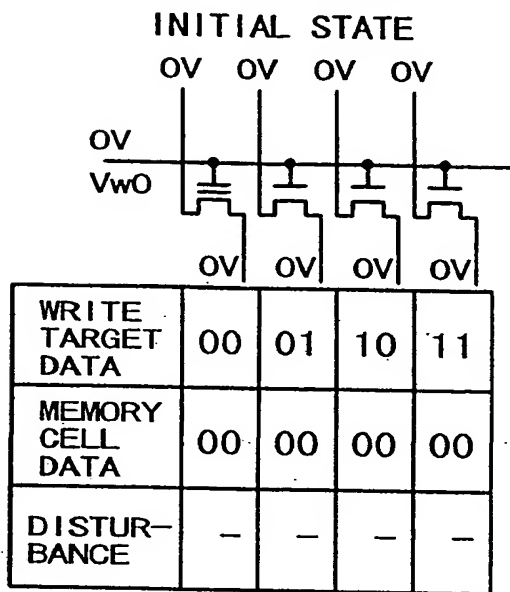


FIG. 3B (PRIOR ART)

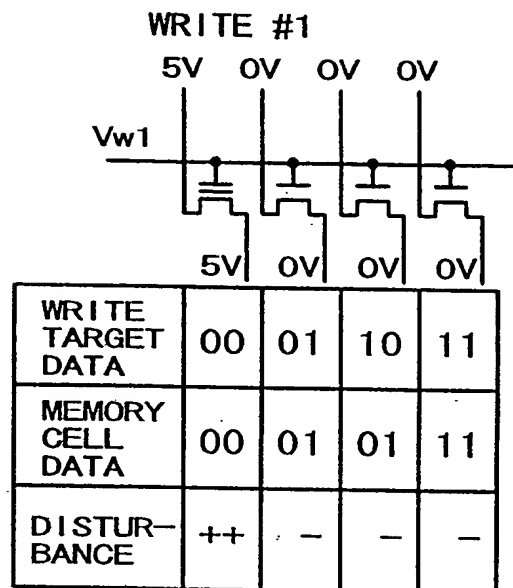


FIG. 3C (PRIOR ART)

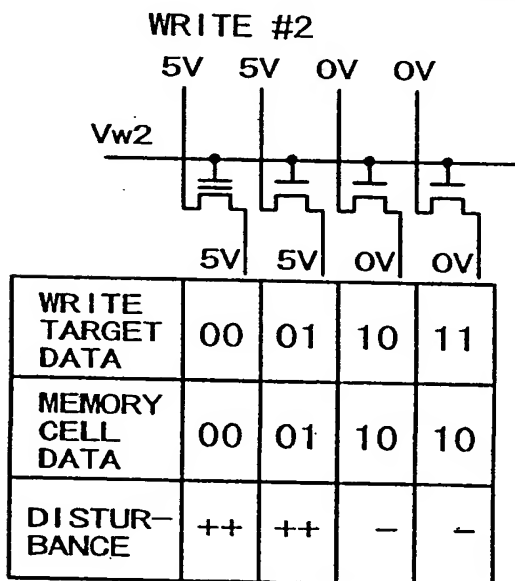


FIG. 3D (PRIOR ART)

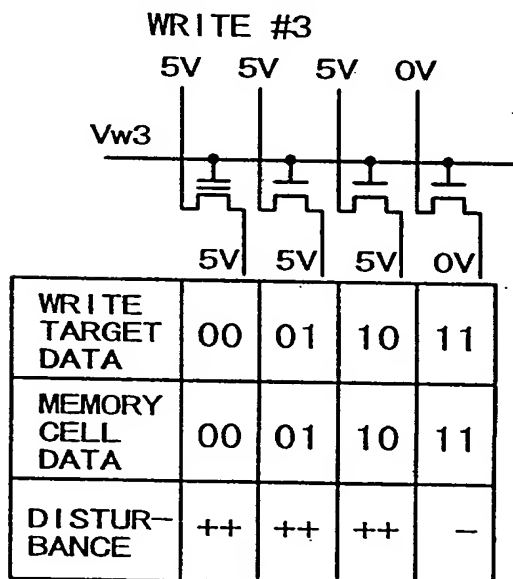


FIG. 3E (PRIOR ART)

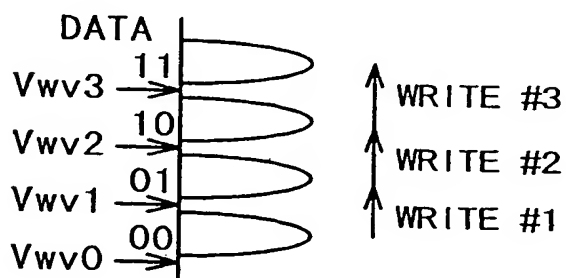


FIG. 4A (PRIOR ART)

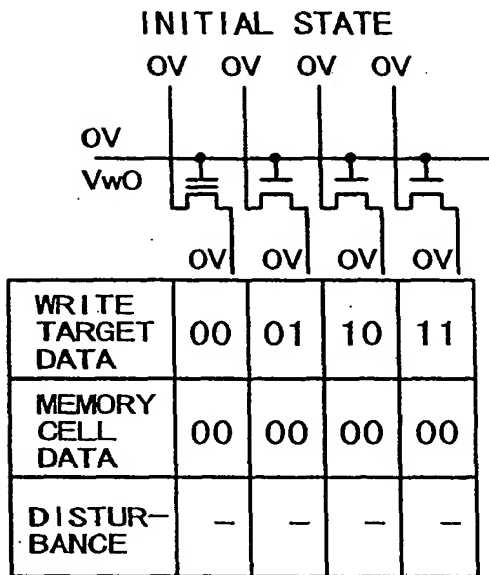


FIG. 4B (PRIOR ART)

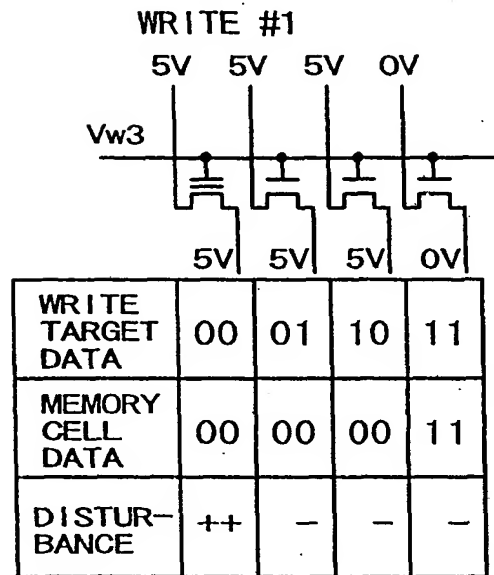


FIG. 4C (PRIOR ART)

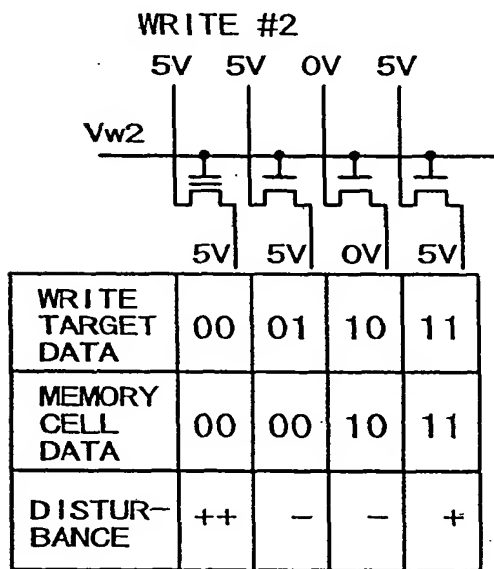


FIG. 4D (PRIOR ART)

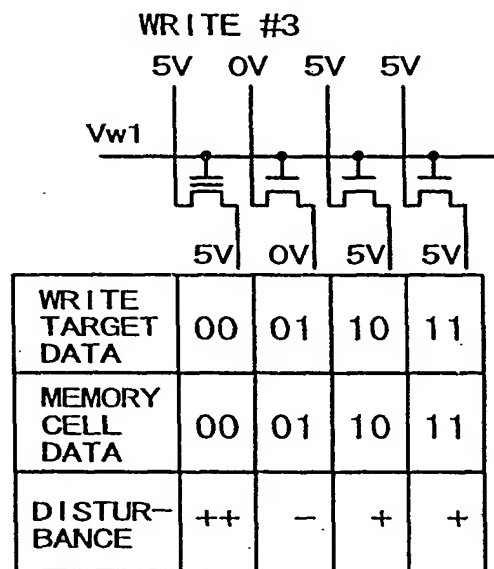
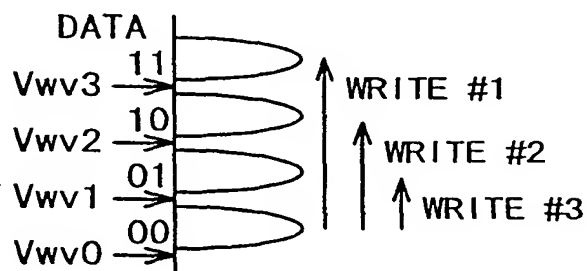


FIG. 4E (PRIOR ART)



The diagram illustrates a cross-sectional view of a memory cell in a 1T1C1D1 architecture. The cell is situated within a p-well (pwell) region, which is separated from the substrate (psub) by a gate oxide layer. The cell structure includes a control gate (CG) and a floating gate (FG) stacked vertically. The CG is connected to a 17/0V supply, while the FG is connected to a 0/5V supply. The cell is surrounded by n+ regions, which are connected to a 0V supply. The cell is also connected to a p+ region, which is connected to a 0V supply. The diagram is labeled "ELECTRON INJECTION (SELECTED CELL)" and "pwell" and "psub".

A schematic diagram of a selected cell for electron emission. The diagram shows a cross-section of a device with a central region labeled "ELECTRON EMISSION (SELECTED CELL)". This region is bounded by a "pwell" and a "psub" (p-substrate). Above the pwell, there are two stacked rectangular regions labeled "CG" (Control Gate) and "FG" (Field Gate). The CG gate is connected to a terminal labeled "10/0V". The FG gate is connected to a terminal labeled "0V". To the left of the CG and FG gates, there is a terminal labeled "0V" connected to an "n+" region. To the right of the CG and FG gates, there is a terminal labeled "5/0V" connected to an "n+" region. Further to the right, there are two "p+" regions, each connected to a terminal labeled "0V".

A schematic diagram of a selected cell for electron emission. The diagram shows a cross-section of a semiconductor device. At the top, a gate stack consists of a Control Gate (CG) and a Field Gate (FG). The CG is connected to a terminal labeled $-17/0V$. The FG is connected to a terminal labeled $0V$. The device is surrounded by a $0V$ potential region. The substrate is labeled $pwell$ and $psub$. The text "ELECTRON EMISSION (SELECTED CELL)" is written in the center of the device.

FIG. 7

	PRESENT INVENTION	PRIOR ART 1	PRIOR ART 2
WRITE #1	1	13	1
WRITE #2	13	21	27
WRITE #3	21	1	13
PULSES	35	35	41

FIG. 8

	PRESENT INVENTION	PRIOR ART 1	PRIOR ART 2
WRITE TIME PERIOD	1449 μ SECONDS	1449 μ SECONDS	1695 μ SECONDS
"00" LEVEL DISTURBANCE	0. 381V	0. 382V	0. 382V
"01" LEVEL DISTURBANCE	0. 001V	0. 097V	0. 000V
"10" LEVEL DISTURBANCE	0. 000V	0. 017V	0. 000V
"11" LEVEL DISTURBANCE	0. 000V	0. 000V	0. 000V

FIG. 9

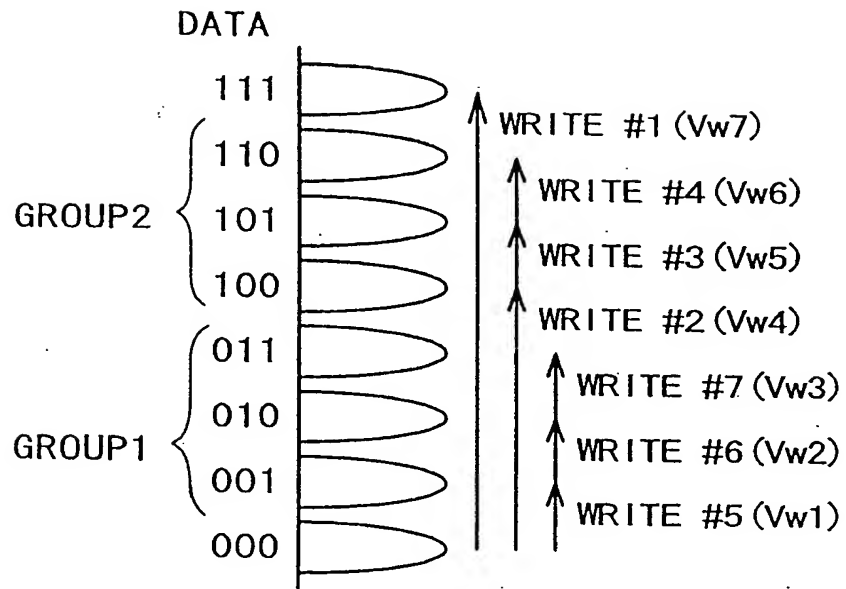


FIG. 10

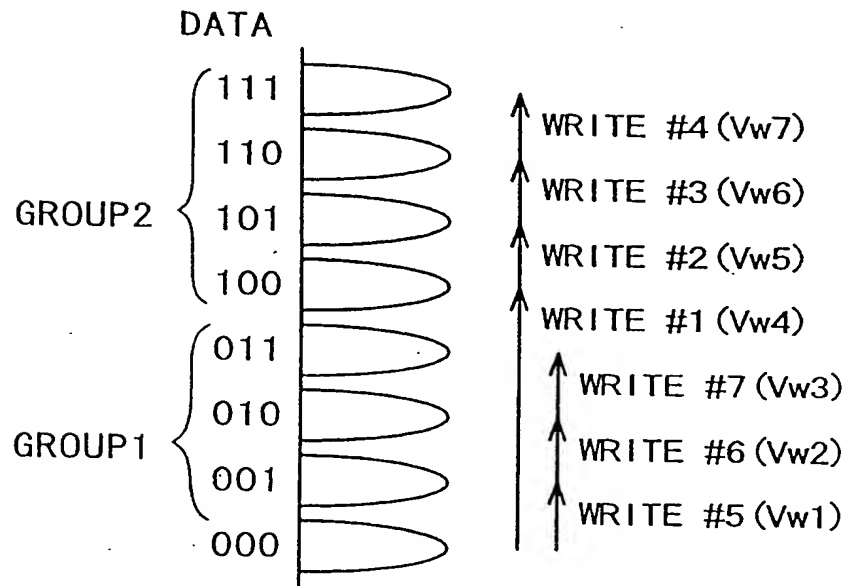


FIG. 11A

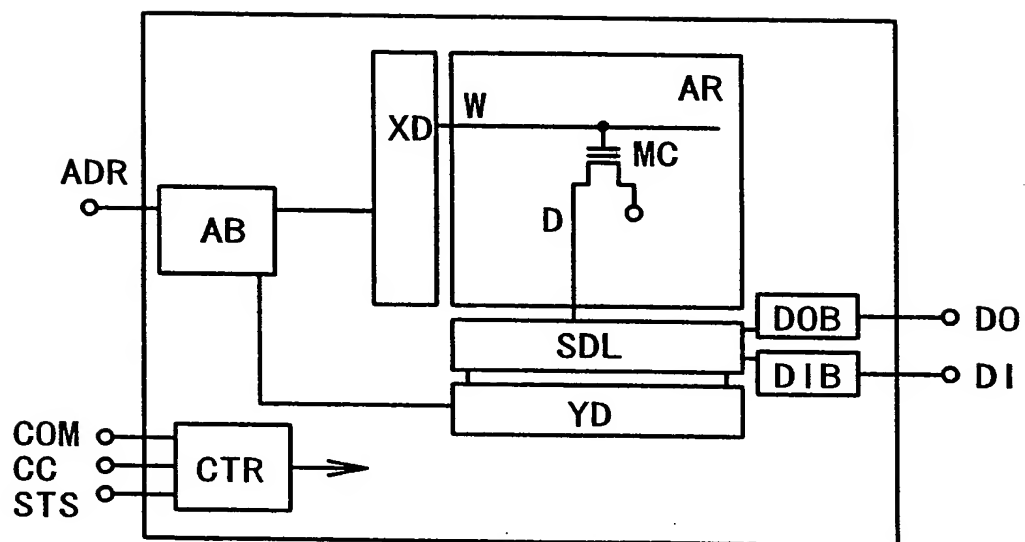


FIG. 11B

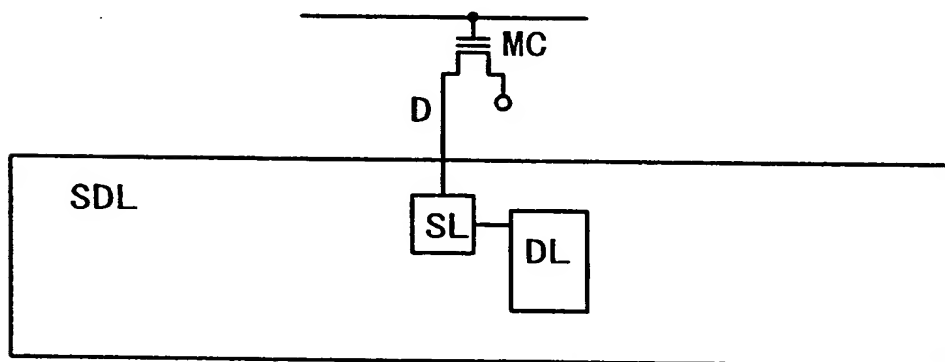


FIG. 12

